Published by IOP Publishing for Sissa Medialab

Received: *July 19, 2021*
Revised: *February 10, 2022*
Accepted: *April 13, 2022*
Published: *May 13, 2022*

TECHNICAL REPORT

Top-down design methodology for a 2 ps rms Jitter at 2.56 GHz of an analog PLL based on Ring and LC Tank Oscillators

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Abstract: A top-down methodology is proposed to design Phase-Locked-Loops (PLL) using behavioural and transistor-level simulation in two cases: Ring-Oscillator (RO) and LC Tank Oscillator (LCTO) with the aim to achieve a low-jitter PLL clock generator in 130 nm process. The optimization of these two PLLs is obtained in three steps. The first one is to design a model in Verilog-A of each block with its intrinsic jitter parameter. Each block is simulated alone to verify the nature of its intrinsic jitter: Frequency Modulation jitter (FM jitter) or Phase Modulation jitter (PM jitter). The second step is to place each of these blocks in a global schematic to obtain a full behavioural PLL. In this way, one can study the PLL operation and check the effect of each block's jitter on the PLL output. The third step is to use the intrinsic FM jitter or PM jitter values to simulate at the transistor level of each block individually and then all of them together. To evaluate the loop bandwidth and the loop stability of each of the two PLLs, a linearized PLL is designed using ideal sources. This approach is important to check the compatibility of each block in terms of jitter and bandwidth with respect to the target PLL performance. The optimization results are used to design and produce two PLLs. Measurements of these two are found to have an absolute time jitter of the order of 2 ps rms.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; VLSI circuits; Modular electronics

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https://doi.org/10.1088/1748-0221/17/05/T05014

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1 Introduction

The aim of this project is to develop a PLL for ASIC developments which integrates time measurement or which requires an internal clock in the range of Gigahertz. For future detectors to be used in High Energy Physic experiments, time measurement becomes a decisive element, which will make it possible to reduce the data flow and to improve the spatial accuracy of the interaction point. For reasons related to background reduction among others, developments in medical imaging also need precise time measurement. Applications based on Time of Flight (ToF) technique such the one used for the Positron Emission Tomography (PET) require time precision around 10 ps for optimal exploitation. Similarly, fast ADC and analogue memory systems also require clock generators with a frequency of up to 2 GHz with jitter smaller than 5 ps rms.

The block diagram of a typical PLL operating as a clock generator is shown in figure 1. It consists of a Frequency reference input (F_{ref}), a Phase-Frequency Detector (PFD), a Charge Pump

(CP) with its output current (I_{cp}), a low pass Loop Filter (LF) with its equivalent impedance (Z_{lp}), a Voltage Controlled Oscillator (VCO) with its conversion gain (K_{vco}) and a Frequency Divider (FD) of 1/N ratio. The feedback is used to equalize the phases of the reference frequency F_{ref} (40 MHz) and the feedback frequency F_{fb} (2.56 GHz). When the PLL is locked, the frequency at the output of the PLL is given by:

$$F_{out} = NF_{ref} \tag{1.1}$$

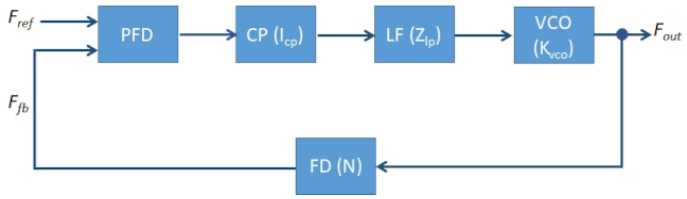

Figure 1. Simplified PLL block schematic.

The loop gain (G_{loop}) based on input phase (Φ_{ref}) and output phase (Φ_{out}) of the signals of the PLL can be written as:

$$G_{loop} = \frac{\Phi_{out}}{\Phi_{ref}} = I_{cp}Z_{lp}(p)\frac{K_{vco}}{p}\frac{1}{N} \tag{1.2}$$

Where p is Laplace Transform variable of the pulsation ω.

We designed two types of PLLs. The first one is based on a Ring Oscillator (RO, PLL_RO) and the second on a LC Tank Oscillator (LCTO, PLL_LC) in order to compare their absolute jitter versus the silicon area needed in each [1–3]. The PLL_RO uses low silicon area compared to the area needed to integrate the self-inductance of the PLL_LC. However, the latter has a higher spectral purity, due to the higher Q factor of LCTO compared to the poor value of the RO's one. Many of the current integrated PLLs use RO as VCO, mainly for its small silicon area. However, the low damping factor (at most equal to $\pi/2$) [4–6] of these oscillators does not permit to achieve low jitter PLL. VCO based on LCTO has damping factors greater than 10, which results in ultra-low jitter PLLs [7, 8]. The main characteristics of the two PLLs developed in this work are listed in table 1. The two share the same parameters except for the K_{vco} as can be seen in this table. This results from the block diagrams of the two PLLs shown in figure 2 where several blocks are common to both.

Table 1. PLL main characteristics.

F_{ref}	40 MHz
F_{out}	2.56 GHz
I_{cp}	50 µA
K_{vco}	1200 MHz/V for PLL_RO 400 MHz/V for PLL_LC
N	64
Phase Margin	65 Deg
Loop Bandwidth	F_{ref}/10
Absolute output jitter	2–3 ps rms

The block diagram for the two PLLs is shown in figure 2.

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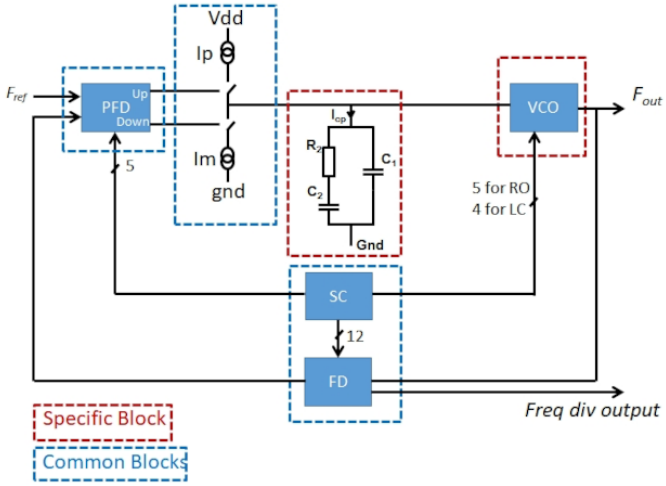

Figure 2. PLL block diagram.

A Slow Control block (SC) is implemented and based on an SPI bus. It sets the configuration bits for the following blocks (table 2):

Table 2. Slow Control configuration bits.

Blocks	Number of bits	Tuning parameter
PDF + CP	12	I_{cp}
VCO_RO	5	Ring Oscillator's bias current
VCO_LC	4	LC Tank Oscillator's capacitance value
FD	12	Selection of the divider intermediate stage test output

2 Behavioural PLL: jitter and loop stability

2.1 Jitter

The term *jitter* could simply be defined as the "deviation of transition edge's time with respect to its ideal one". Several metrics are used in the literature depending on how the notion of "ideal time" is defined.

The definition implies a choice of the edge direction (either the rising or the falling one, here after we opt for the rising one) and a statistical set of such transition edges. When dealing with a clock, the statistical set is the discrete-time series of time deviations for all successive chosen edges. That statistical time series can be analysed in terms of Probability Distribution Function (PDF) and standard deviation. When characterizing a PLL, the jitter should also be analysed like any discrete-time signal for more information on the time structure of the jitter, e.g. to detect modulation patterns. Such analysis includes visualizing the jitter vs time, in simulation or measurements using oscilloscopes having adequate characteristics or spectrum analyser. It can also include frequency-domain analysis via Fourier Transform.

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The simplest jitter metric for a periodic signal is the "period jitter". It quantifies the deviation of the period with respect to its average value (T) as follows:

$$J_{\text{per}} = \text{stdev}(t[n] - t[n-1]) \tag{2.1}$$

Where stdev denotes the standard deviation.

An "absolute jitter" is another way of evaluating the jitter. It is the deviation of the edge time with respect to that of an ideal periodic clock, having the same average period and phase:

$$J_{\text{abs}} = \text{stdev}(t[n] - nT) \tag{2.2}$$

In PLL design for timing application, the absolute jitter is the jitter key parameter. The different types of jitter in a PLL are classified according to their origin [8]. PFD, CP and FD exhibit synchronous jitter because they are driven circuits. This type of jitter is called "Phase-Modulation" (PM) jitter because the noise added to the signal modifies the instantaneous phase. Since the system is driven by an external stimulus, the phase deviation is bounded. On the other hand, VCO exhibits a cumulative jitter because it is an autonomous circuit. Noise sources cause modulations of the oscillation frequency hence the notion of "Frequency-Modulation" (FM) jitter. Since the oscillator is autonomous, the deviations occurring cycle after cycle have a cumulative effect on phase.

A behavioural model of PLL in Verilog-A has been designed in order to evaluate the impact of each block's jitter on the final output jitter using transient simulations. The model is also used to optimize the PLL design to meet the specifications [9]. The final output jitter is well characterized by the period jitter (J_{per}) and the absolute jitter (J_{abs}) defined before. In the case of clock synthesis design, the contributions of the VCO and the PFD_CP are the most important in terms of jitter optimization. Table 3 gives the simulation results, they are valid for the two kinds of PLLs since the stability criteria for both are the same although the gains of the VCOs are different. In the case where all individual jitters are equal to zero, J_{per} and J_{abs} should be, in principle, equal to zero. An increase of time precision of both the Verilog-A model and the simulator allows J_{per} and J_{abs} to reach the asymptotic value of zero provided a long simulation time. A trade-off should be found between jitter results and simulation time. Apart from the VCO and the PFD_CP, the simulation imprecision can lead to an additional jitter if the simulator time step is not fine enough (of the order of a few tens of femtosecond).

Table 3. PLL behavioural simulations.

FM jitter VCO [fs rms]	PM jitter FD [fs rms]	PM jitter PFD-CP [fs rms]	Output J_{per} [fs rms]	Output J_{abs} [fs rms]
0	0	0	few fs	few fs
60	0	0	59.2	949
0	200	0	0.65	138
0	0	300	0.76	153

The Verilog-A PFD_CP model does not include the positive and negative output current pulses when the PLL is locked. It is a key point for the absolute output jitter and for a non-dead zone PDF_CP. Additionally, the PFD_CP Verilog-A simplified model induces jitter only during the

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locking time. These two characteristics explain the fact why the absolute output jitter J_{abs} value is in the range of a hundred femtoseconds (153 fs in table 3) when only the jitter of the PFD_CP is taken into account.

We used a top down design procedure to implement the two types of PLLs:

1) Compute the loop filter as described below and define the cut off frequency f_L of the loop transfer function as described in [10, 11]. The f_L frequency is defined by the zero of the loop filter.

2) Compute κ and c values [13], which make the link between the VCO open loop jitter and the closed loop output PLL absolute jitter (J_{CL}). These two parameters are also a FOM (figure Of Merit) to compare PLLs.

$$\kappa = \frac{J_{CL}}{\sqrt{2}}\sqrt{4\pi f_L} \tag{2.3}$$

$$c = \kappa^2 \tag{2.4}$$

3) Compute the VCO period jitter (J_{per}).

$$J_{per} = \sqrt{\frac{c}{F_{out}}} \tag{2.5}$$

4) Compute L(Δf), the Single Side Band (SSB) phase noise as a function of the offset carrier frequency Δf.

$$L(\Delta f) = \frac{cF_{out}^2}{\Delta f^2} \tag{2.6}$$

and its expression $L'(\Delta f)$ in dBc/Hz.

$$L'(\Delta f) = 10 \cdot \log_{10}(L(\Delta f)) \tag{2.7}$$

Δf must be chosen well above the corner frequency (Fc) of the VCO phase noise and below F_{out} to avoid VCO flicker noise. Therefore, the VCO white noise will be dominant. For the two VCOs, the corner frequency is 1 MHz which is determined by the technology of 130 nm CMOS we propose to use.

5) VCO optimization is obtained by simulating $L'(\Delta f)$ and J_{per} based on the SpectreRF simulator. $L'(\Delta f)$ is obtained at 4 MHz for RO and for LCTO by modifying the transistors geometry to reach the lowest noise. This value of 4 MHz corresponds to the Loop Bandwidth of these two PLLs. In both PLLs, a Closed Loop absolute jitter (J_{CL}) in the range of 1–3 ps rms can be reached. The PLL features obtained with this optimization procedure are listed in table 4. The constraints on the transistor size and the bias current determine the optimal J_{CL} value one would like to have. Depending on the constraints, one may opt for one architecture or the other.

J_{per} and $L'(\Delta f)$ are the key features of the VCOs and their values determine the final performance of the two PLLs. The final target is to design VCOs with J_{per} lower than 100 fs rms and $L'(\Delta f)$ lower than -110.4 dBc/Hz at 4 MHz offset frequency from carrier to reach the 2 ps performance.

6) PFD_CP optimization based on transient noise simulations and SpectreRF simulator to reduce its phase noise. The optimization of this results is a phase noise lower than - 144 dBc/Hz at 4 MHz offset frequency with respect to the carrier's one.

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Table 4. PLLs features associated to VCO jitter optimization.

J_{CL} [ps rms]	k [$\sqrt{s}$]	J_{per} [fs rms]	$L'(\Delta f)$ [dBc/Hz]
1	2.36E−9	46.63	−116.42
2	4.72E−9	93.26	−110.40
3	7.08E−9	139.90	−106.88

2.2 Loop stability

A linearized model is designed to study and verify the loop stability as a function of the key features of the PLL (table 1) and the loop filter design. The loop filter converts the output current of the charge pump into a voltage.

The most commonly loop filter (figure 3) used in analogue PLL is made of two capacitors (C_1, C_2) and a resistor (R_2).

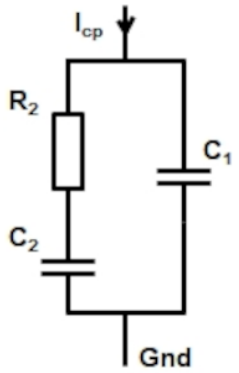

Figure 3. Loop filter schematic.

By setting a phase margin Φ_M and a cut-off frequency ($f_c = \omega_c/2\pi$) for which the loop gain (G_{loop}) is 0 dB, one can calculate the component's values [12] of the loop filter as follows:

$$C_1 = \frac{\omega_z}{\omega_p}\frac{I_{\text{cp}} 2\pi K_{\text{vco}}}{\omega_c^2 N}\frac{\sqrt{1+(\frac{\omega_c}{\omega_z})^2}}{\sqrt{1+(\frac{\omega_c}{\omega_p})^2}}, C_2 = C_1\left(\frac{\omega_p}{\omega_z}-1\right), R_2 = \frac{1}{C_2\omega_z}, \text{ with } \omega_p = \frac{\omega_c}{\frac{1}{\cos\Phi_M}-\tan\Phi_M}, \omega_z = \frac{\omega_c^2}{\omega_p} \tag{2.8}$$

A key design criterion for a PLL, is to set f_c to 1/10 of F_{ref} [12] (40 MHz in our case) to ensure good phase margin. This ratio can be optimized if the PLL acts as jitter cleaner or clock generator. The output phase noise referred to the F_{ref} phase noise has a low pass behaviour and the output phase noise referred to the VCO phase noise has a high pass behaviour. The choice of f_c is a trade-off between two conflicting targets: filtering F_{ref} phase noise or minimizing VCO cumulative jitter. Therefore, in the case of the PLL acting as a cleaner jitter (clock generator) the PLL cut-off frequency must be as low (high) as possible respectively, ensuring a good phase margin. This design is made in the context of a clock generator. The jitter of F_{ref} is assumed to be small enough in order to have a negligeable effect on the PLL output phase noise. The values of the loop filter components in both cases, using the previous formula, are given in table 5.

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Table 5. PLLs loop filter parameters.

	R_2 [kΩ]	C_2 [pF]	C_1 [fF]
PLL_LC	84	2.1	110
PLL_RO	28	6.4	330

Since all parameters of the two PLLs are identical, except the VCO gain, f_p, f_c and f_z are consequently the same. They are respectively 18 MHz, 4 MHz and 886 kHz.

3 Common blocks

3.1 PFD-CP

The function of the PFD is to generate a voltage controlled by the difference in phase between the reference clock and the PLL output clock to ensure that the output and input clock have a constant difference in phase.

Thus, this block provides control signals to the charge pump driving the input of the VCO. When the phase difference is positive (negative) the charge-pump voltage is decreased (increased) respectively. In order to reduce the noise voltage, which will be transformed into jitter, the comparator is based on a "no dead zone" structure minimizing jitter. This concept consists in generating both "up" and "down" signals independently of the phase difference and even if the clock signals are in phase. It permits to avoid an operating range in which the feedback system is uncontrolled and thus in an open-loop state.

So, the phase and frequency detector illustrated below (figure 4 and figure 5) [14, 15], allows the delivery of respectively two outputs signals "up" and "down" where the duration is proportional to the phase difference between the two inputs "F_{ref}" and "F_{fb}".

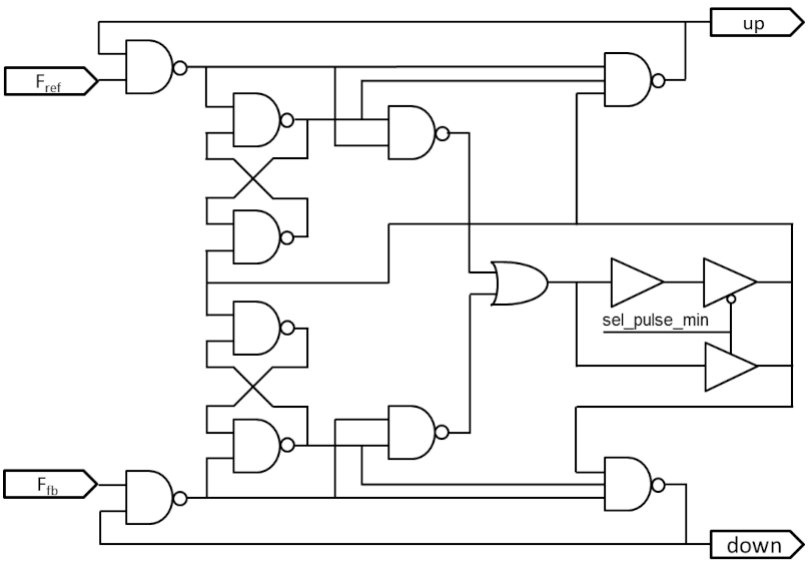

Figure 4. Classical structure of a no dead zone phase and frequency detector.

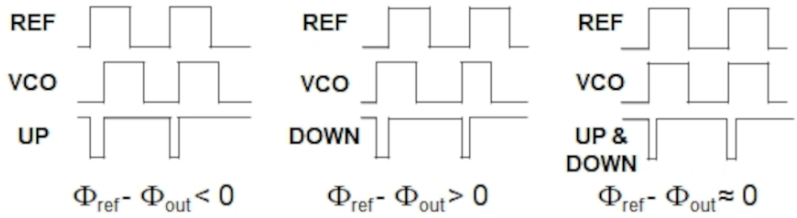

Figure 5. Chronograms of a no dead zone phase and frequency detector.

The PFD block is designed with a reset system, which initializes the logic part and sets a minimal pulse duration for "up" and "down" signals when the PLL is locked.

The "charge pump" cell (figure 6) allows the injection of charges into the loop filter proportionally to the duration of the "up" and "down" signals. The charge pump uses a differential structure which minimizes charge injection. As presented in figure 6, the charge pump is controlled by an external current source which drives both PMOS and NMOS current sources loading the loop filter. To optimize the phase error, these current sources are tuneable by 5 bits of the SC parameters (in/ip0 to in/ip4 in figure 6).

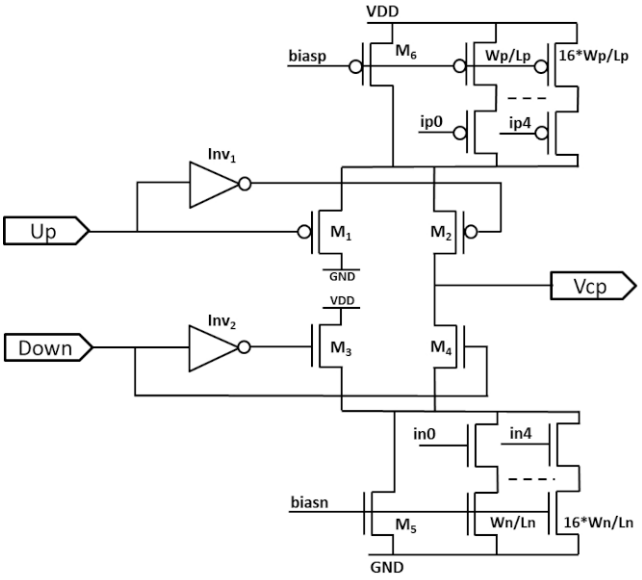

Figure 6. Schematic of the tuneable charge pump structure.

Once the phase difference between the reference input clock and the PLL output is constant, the peak in DC voltage at the PFD_CP output is 4 mV during 200 ps. This change in voltage comes from the phase shift between up and down signals and the response time of $\text{Inv}_{1\text{–}2}$–$M_{1\text{–}4}$. It has no effect in terms of jitter on the VCO output since it is out of the VCO bandwidth used in the two PLLs. Spurious in phase noise could appear but it cannot be seen in transient noise simulation of the two PLLs. Additionally, the drain of M_1 and M_3 was initially connected together. By opening this node and connecting them to GND and VDD, the current of $M_{5\text{–}6}$ can be adjusted separately and then reduce the PLL phase noise.

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It is worth mentioning here that also, as can be seen in table 3, the jitter due to the PFD_CP is small. In the case of a MOS transistor PFD_CP implemented in a no phase noise behavioural PLL, the absolute output jitter due to the PFD_CP could be higher and reach a value as high as 660 fs rms. In our simulation, the effective value of the PFD_CP jitter is taken into consideration in an appropriate way.

3.2 Frequency divider

The purpose of the frequency divider here is to divide the output frequency by a ratio of 64, so that the phase of the PLL output can be compared to the phase of the input signal.

The two critical points of this frequency divider are its operating frequency (2.56 GHz) as well as the low jitter desired in the PLL. Several solutions have been considered to design the frequency divider. Synchronous and asynchronous dividers were compared for the targeted applications. The solution that best meets the requirements of low jitter is the use of an asynchronous divider. This kind of architecture is implemented in the two PLLs. The architecture is composed of 6 D type Flip-Flop. All the Flip Flop are standard cells. To improve the jitter of the divider, a resynchronization of F_{out} with the reference signal has been added [16, 17]. The simulation results show an absolute output jitter of 129 fs rms.

4 PLLs implemented

4.1 PLL_RO

4.1.1 Ring Oscillator

The VCO architecture is based on a differential inverter where polarization current is variable. It allows the control of the inverter's delay and therefore the oscillation frequency (F_{osc}) of the RO. The oscillation frequency is inversely proportional to the propagation delay (t_d) of an inverter and to the number (n) of inverters implemented in the RO.

$$F_{\text{osc}} = \frac{1}{2nt_d} \tag{4.1}$$

The differential structure (figure 7) is chosen for the following reasons:

- It limits the noise injected by the power supplies.
- It sets a constant current seen from power supplies.
- It is possible to use an even or odd number of inverters in the RO in order to optimize the output frequency and the jitter.

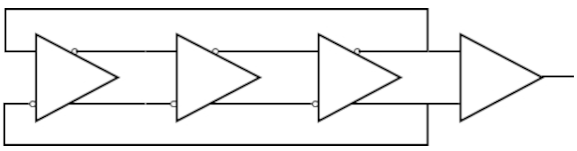

Figure 7. Typical three stages differential Ring Oscillator.

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A differential-to-single-ended stage is added at the output of the RO to shape and drive the single ended frequency divider.

A default inherent in VCOs and therefore in RO is the cumulative jitter. In RO, the cumulative jitter depends on the jitter of an inverter and the number of inverters that make the RO. Several differential structures were simulated, a trade-off was made on the number of inverters and the propagation delay of an inverter in order to obtain an oscillation frequency of 2.56 GHz for a control voltage of 600 mV ($n = 3$ and $t_d = 65$ ps).

The selected differential inverter architecture is similar to those proposed in [18, 19]. This architecture is chosen for its simplicity and low phase noise. The positive feedback reduces the rise and fall time of the signals and therefore reduces the final jitter. The schematic of the differential inverter ([18, 19] and figure 8) is optimized for an oscillation frequency of 2.56 GHz.

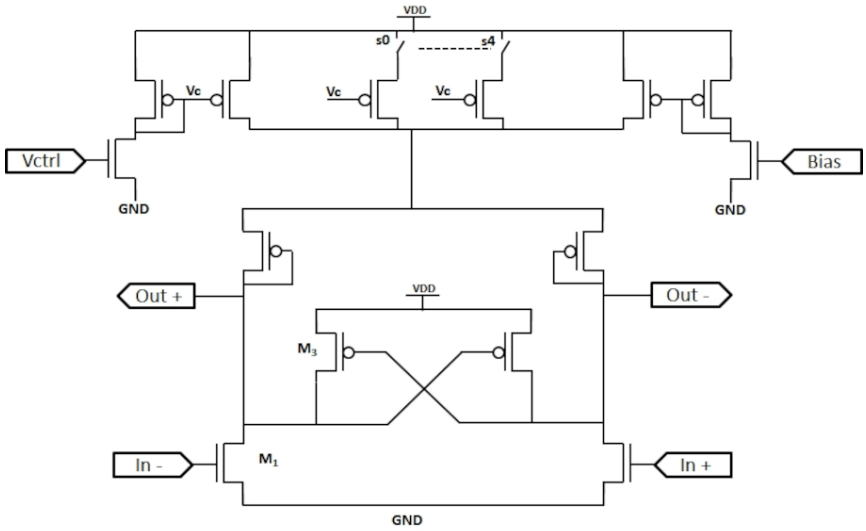

Figure 8. Full schematic of the tuneable differential buffer.

The output frequency is a function of the NMOS differential pair transconductance, the PMOS cross pair transconductance and the capacitive output load C_L. Therefore, $F_{\min}$ and $F_{\max}$ define the frequency dynamic range.

$$F_{\min} \sim \frac{1}{2\pi}\sqrt{\frac{g_{mM1}^2 - g_{\mathrm{mM3}}^2}{C_L^2}} \tag{4.2}$$

$$F_{\max} \sim \frac{1}{2\pi}\frac{g_{\mathrm{mM1}}}{C_L} \tag{4.3}$$

Five bits of the SC parameters (s0 to s4 in figure 8) are implemented to increase the bias current mirror in order to take into account the process variations.

In addition, the behaviour of the cumulative jitter as a function of the number of edges is in accordance with theory. VCO optimization is based on the Periodic Steady State (PSS) and the Periodic noise (Pnoise) simulation tools. The Pnoise simulation returns the noise contributors. The VCO optimization gives the following result: $L'(\Delta f) = -113.125$ dBc/Hz at 4 MHz. This level of phase noise, according to the formalism of Ken Kundert [8] gives a constant c value of $6.3 \cdot 10^{-18}$ s.

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Furthermore, the VCO period jitter (J_{per}) is found to be 49.7 fs rms and so, the absolute output rms closed loop jitter is 1.1 ps rms. The main performances of the VCO_RO alone are listed in table 6.

Table 6. Typical simulation performances of the VCO_RO.

K_{vco}	1000 MHz/V
Power	7.8 mW
Fmin-Fmax	2.3 GHz–2.9 GHz

4.1.2 Ring Oscillator in PLL_RO

The PLL_RO simulations were carried out by gradually adding the real blocks with MOS transistors in a behavioural PLL schematic. The result of transient noise simulation for the full PLL_RO in MOS transistors is listed in the table 7. Jitter results can be easily calculated from formula(2.3) to (2.5) and are in good agreement with simulations.

Table 7. PLL_RO transient noise simulation results.

Output frequency	2.56 GHz
Locked time	2 µs
Input VCO voltage	610 mV
Output absolute jitter	1.4 ps rms
Output period jitter	65 fs rms

4.2 PLL_LC

4.2.1 LC Tank Oscillator

The VCO architecture used in this work is based on a LCTO topology which is qualified for resonant oscillator.

A control voltage V_{ctrl} in input is applied to the VCO to define the output frequency F_{out}, which is directly proportional to the control voltage. The frequency range of the oscillator can be tuned by the system specification using four bits (s0 to s3 in figure 9) of the SC parameters, additional margin is required to cover process and temperature variations. The frequency spectrum of the LCTO is broadened by the noise of its components. The magnitude of phase noise is a trade-off between tuning range and power dissipation of the oscillator. The oscillator is viewed as an RLC circuit. The design must have a negative phase margin to ensure oscillations. In fact, the oscillation is damped due to the presence of the parasitic resistance R_p of the self-inductance L. A negative resistance must be implemented to compensate the R_p component.

The oscillation frequency is defined by:

$$F_{out} = \frac{1}{2\pi\sqrt{LC}} \tag{4.4}$$

Practically, the design of the LCTO is composed of a symmetrical inductance [20, 21], a varactor and a pair of NMOS and PMOS cross-coupled transistors (figure 9). The value of the inductance is 1.4 nH with a quality factor of 11. The tuning range of the varactor is set between 0.8 pF to 2.5 pF.

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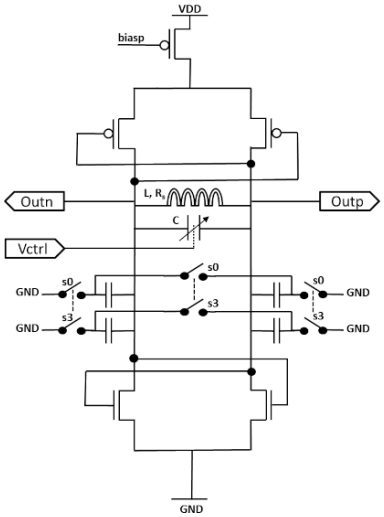

Figure 9. Full schematic of the tuneable VCO_LC.

The quality factor Q of the symmetrical self-inductance is defined by:

$$Q = \frac{Lw}{R_s} = \frac{R_p}{Lw} \tag{4.5}$$

with

$$R_p = \frac{(Lw)^2}{R_s} \tag{4.6}$$

The cross-coupled oscillator must validate the following conditions to ensure oscillations:

$$g_m R_p > 2 \tag{4.7}$$

where g_m is the PMOS cross-coupled transconductance.

The output voltage V_{out} is proportional to the bias current I_{ss}:

$$V_{\text{out}} \sim R_p I_{ss} \tag{4.8}$$

In terms of design, two parameters play an important role to limit the noise. Q must be as high as possible and the bias current as large as is allowed for power dissipation specifications. A capacitor bank, controlled by SC, is also implemented to tune the frequency oscillation (s0 to s3) in order to take into account the process variations. The minimum and the maximum frequency oscillation are defined as this:

$$F_{\text{max}} = \frac{1}{2\pi} \frac{1}{\sqrt{L(C + C_{\text{min}})}} \tag{4.9}$$

$$F_{\text{min}} = \frac{1}{2\pi} \frac{1}{\sqrt{L(C + C_{\text{max}} + nC_u)}} \tag{4.10}$$

where C_{max}, C_{min} are respectively the upper and lower value of the capacitor C range and nC_u an additional capacitor controlled by s0 to s3.

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The resistance of the closed switch degrades the Q factor of the LCTO. There is a trade-off between the Q and the tuning range implemented. The switches in the capacitor banks are implemented using a set of 3 switches (figure 9) in order to reduce their equivalent parasitics resistance. Only a third of the switch resistance appears in series with each capacitor, the impact on the Q factor is limited. In our case, we implemented a frequency tune between 2.1 GHz and 3.1 GHz.

The VCO optimization gives the following result: $L'(\Delta f) = -117.3$ dBc/Hz at 4 MHz. This level of phase noise, according to the formalism of Ken Kundert gives a constant $c = 4.5 \cdot 10^{-18}$ s [8]. Furthermore, the VCO period jitter (J_{per}) will be 42 fs rms and so, the absolute output rms closed loop jitter is 900 fs rms. The main performances of the VCO_LC alone are listed in table 8.

Table 8. Typical simulation characteristics of the VCO_LC.

K_{vco}	350 MHz/V
Power	6 mW
Fmin-Fmax	2.1 GHz–3.1 GHz

4.2.2 LC Tank Oscillator in PLL_LC

The PLL considered here is composed of 6 components represented in figure 10. Compared to figure 1 of a classical PLL, an amplifier based follower is added to isolate the loop filter from the large VCO input capacitance (figure 10). This allows keeping the same architecture of charge pump in the two PLLs design.

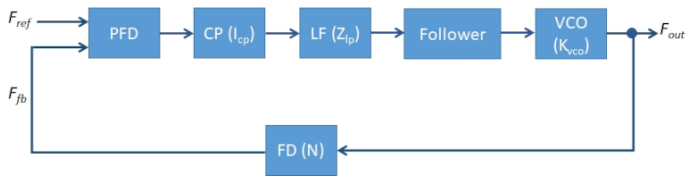

Figure 10. Synoptic of the PLL_LC.

The main performances of the PLL_LC are listed in table 9. As in the case of RO, jitter results can be easily calculated from formula (2.3) to (2.5) and are in good agreement with simulations.

Table 9. PLL_LC transient noise simulation results.

Output frequency	2.56 GHz
Locked time	2 µs
Input VCO voltage	600 mV
Output absolute jitter	900 fs rms
Output period jitter	40 fs rms

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5 Test results

5.1 Test methodology

The test setup for this design is based on an ultra-low jitter clock generator with 14 programmable outputs from Texas Instrument (LMK386). This allows us to inject a low jitter 40 MHz clock in both PLLs and then to measure the jitter of the two designed PLLs.

In the two cases, the first part of the characterisation consists in studying the VCO output frequency as a function of its voltage input control. Several curves can be obtained by the SC selection bits. The jitter measurement in rms values was done in two different ways.

First, we use a Lecroy oscilloscope with high bandwidth (3.5 GHz) and high sample rate (up to 40 Gs/s). This method allows us to:

- Measure the phase noise in dBc/Hz as function of the frequency offset (Δf) from the carrier frequency (F_{car}) and to calculate the jitter phase noise called J_{PN} defined by:

$$J_{\text{PN}} = \frac{1}{2\pi F_{\text{car}}} \sqrt{2 \cdot \int 10^{\frac{L(f)}{10}} \cdot \Delta f} \tag{5.1}$$

- Measure the Time Interval Error (TIE) as a function of time and then calculate the jitter from the standard deviation of TIE called $J_{\text{sdev(TIE)}}$ here after.

  TIE is defined as:

$$\text{TIE}_n = t_n - \tau_n \tag{5.2}$$

  It is the difference between the observed edge time (t_n) and the expected edge time (τ_n) for each edge present in the clock.

- Calculate the random jitter using the Serial Data Analyser tool (SDAII) called $R(j)_{\text{sdaii}}$ here after.

The second step consists in recording the PLL output signal from the Lecroy oscilloscope and then perform an off-line analysis, based on the FFT of absolute jitter, to extract three distinct jitter components:

- Peaks at frequencies that are multiple of 40 MHz contribute to the total jitter by $J_{40\,\text{MHz\_offline}}$.
- For RO version only, peaks caused by parasitic coupling from the open-loop VCO block result in the so-called $J_{\text{parasitic\_offline}}$.
- The continuous spectrum defines the random jitter contribution: $J_{\text{random\_offline}}$.

The examination of the different contributions to jitter allows the variation interval of the PLL absolute rms output jitter (J_{abs}) to be:

$$J_{\text{random\_offline}} < J_{\text{abs}} < J_{\text{sdev(TIE)}} \tag{5.3}$$

The two measurement methods are consistent:

$$J^2_{\text{random offline}} + J^2_{40\,\text{MHz\_offline}} + J^2_{\text{parasitic\_offline}} = J^2_{\text{sdev(TIE)}} \tag{5.4}$$

$$J_{\text{random\_offline}} = R(j)_{\text{sdaii}} \tag{5.5}$$

The overall output phase noise transfer function of a PLL is a low pass filter. At frequency offset that are two or three times the F_{ref} input, the phase noise could reach -120 dBc/Hz, which is negligible when converted in absolute jitter. Observed peaks at higher frequency are due to internal coupling, that will be discussed later. These peaks are most probably caused by imperfect layout design, in particular at the level of the divider.

5.2 Oscillator test results

Figure 11 and figure 12 show the VCO frequency output as a function of the input control voltage for all SC configurations.

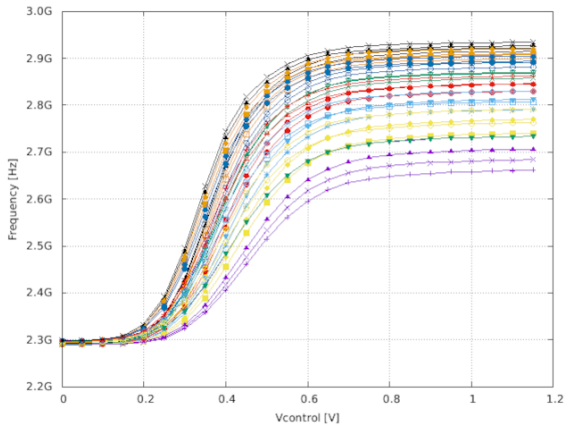

Figure 11. Ring Oscillator F_{out} vs input control voltage.

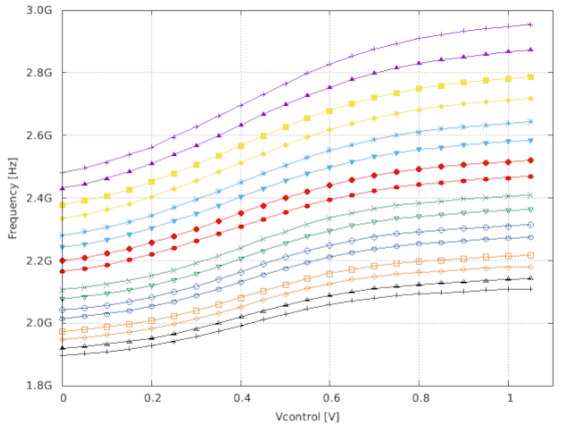

Figure 12. LC Tank oscillator F_{out} vs input control voltage.

The minimum and maximum K_{vco} value in both cases are summarized in table 10.

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Table 10. K_{vco} dynamic range.

	K_{vco} min (MHz/V)	K_{vco} max (MHz/V)
LC Tank Oscillator	340	640
Ring Oscillator	900	2200

In order to measure the jitter of the associated PLL, the VCO SC configuration is set with respect to the loop filter optimisation. The value is set to 640 MHz/V for the PLL_LC and 1000 MHz/V for PLL_RO.

5.3 PLL test results

The bandwidth of the differential output driver is 1.5 GHz and therefore the maximum output divider frequency recordable is 1.28 GHz since higher frequencies are beyond the 1.5 GHz.

For the two PLLs, the output phase noise divider from 40 MHz to 1.28 GHz is shown on figure 13 and figure 14 respectively. As predicted, all the curves are separated by 6 dB. For both PLLs, we observe peaks at frequencies that are multiple of 40 MHz as well as some other frequencies. Indeed, For the PLL_RO only, we observe additional peaks at frequencies that are not multiple of 40 MHz. For example, a peak of the phase noise distribution at 12 MHz can be seen in figure 13. This frequency (and its multiples) proved to be related, via aliasing, to the frequency of standalone VCO divided output (628 MHz in the case of figure 13). So, a change in the standalone VCO divided output or its voltage control input will modify the additional peak frequency. Unfortunately, the VCO standalone RO cannot be stopped, contrary to the VCO LCTO. This is why we decided to separate the components by offline FFT analysis.

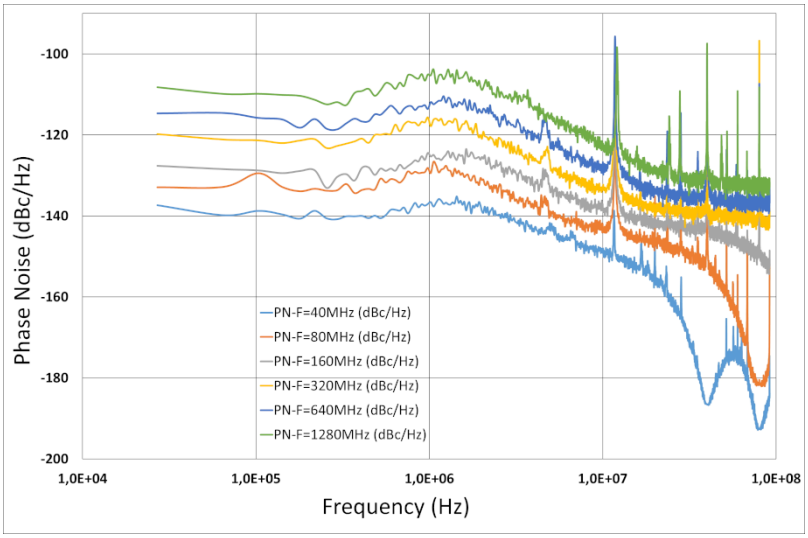

Figure 13. PLL_RO phase noise vs offset carrier frequency.

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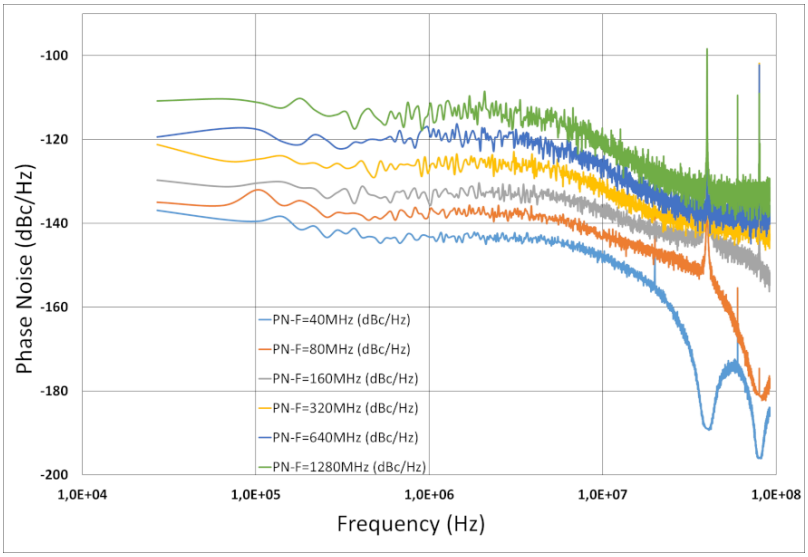

Figure 14. PLL_LC phase noise vs offset carrier frequency.

An offline analysis at 1.28 GHz is performed for the two PLLs (figure 15 and figure 16). In these two figures, the total output jitter as a function of the offset frequency carrier is presented.

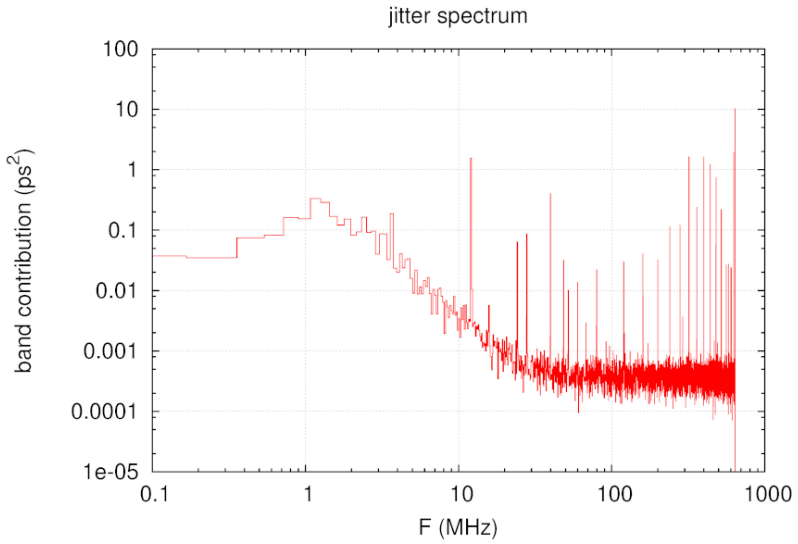

Figure 15. PLL_RO output jitter vs offset carrier frequency.

These two sets of curves feature the same behaviour. At 1.28 GHz, all the contributions of individual jitter in ps rms are listed in table 11. These measurements are well described by the relations given in the previous paragraph.

The final absolute jitter at 2.56 GHz for both PLL in ps rms can be extrapolated from the one at 1.28 GHz because $J_{\text{sdev(TIE)}}$ and $J_{\text{random\_offline}}$ reaches an asymptotic value. These values and listed in the table 12.

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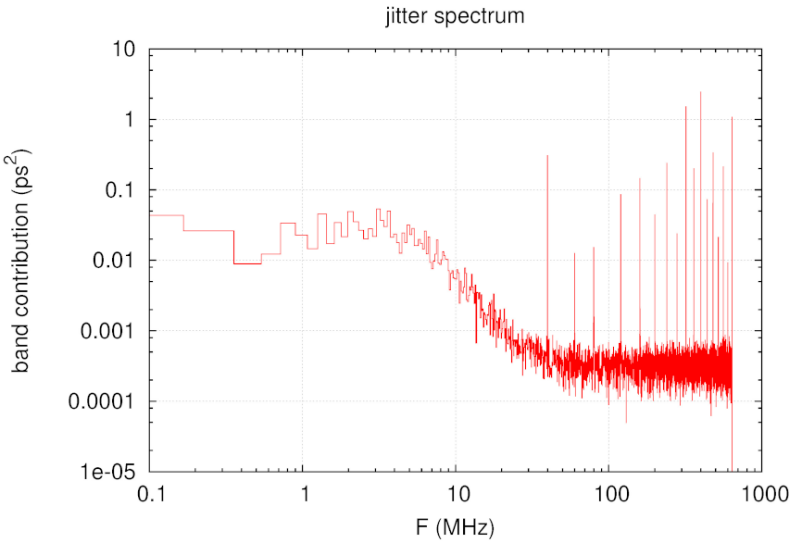

Figure 16. PLL_LC output jitter vs offset carrier frequency.

Table 11. Jitter measurement summary.

	J_{PN}	$J_{\text{sdev(TIE)}}$	$R(j)_{\text{sdaii}}$	$J_{\text{random\_offline}}$	$J_{\text{40 MHz\_offline}}$	$J_{\text{parasitic\_offline}}$
PLL_RO	1.9	5.03	2.05	2.14	4.11	1.93
PLL_LC	1.25	3.1	1.6	1.59	2.62	0

Table 12. Final jitter PLLs limits.

	Lower limit [ps rms]	Upper limit [ps rms]
PLL_RO	2.05	5.03
PLL_LC	1.6	3.1

5.4 Discussion

The jitter components at frequencies multiple of 40 MHz should be filtered out drastically by the loop filter. We observed a predominance of peaks at frequencies 40 MHz, 80 MHz, 160 MHz and 640 MHz (depending on the chosen divider stage). For instance, when we measure the 1.28 GHz, the peak at 640 MHz is dominant in rms jitter integration. This fact points to some parasitic feedback in the divider chain, i.e. a perturbation of "upstream" stages by "downstream" ones. By optimising the layout divider stage, we could then hope to improve the overall jitter performance and being closer to the extracted random component.

A key point in PLL design is the PLL core area and power consumption when this block is implemented in a multichannel front-end ASIC. The core area and the total power consumption of the two PLLs estimated from the simulation are summarized in table 13.

The extra power consumption for the PLL_LC is due to the amplifier-based follower which isolate the loop filter from the VCO_LC.

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Table 13. PLLs core area and power consumption.

	PLL_LC	PLL_RO
Area [sq mm]	0.153	0.052
Power [mW]	9.5	9

Considering the jitter figure of Merit (FoM_j) defined as follow:

$$\mathrm{FoM}_j = 10\log_{10}((\frac{J_{\mathrm{abs}}}{1\,s})^2(\frac{\mathrm{Power}}{1\,\mathrm{mW}})) \tag{5.6}$$

The FoM_j of PLL_RO and PLL_LC are respectively -226 dB and -224 dB. These two designs are within the state-of-the-art performances [22] and are well in accordance with the goal of this development as presented in table 1.

From this work, table 14 demonstrates the trade-off among two PLLs with different VCO architectures and show the pros and cons of the two PLL.

Table 14. Trade-off of PLL_RO and PLL_LC.

	PLL_RO	PLL_LC
Advantages	- Silicon area used - Easy to translate in other process - Could be implemented in digital process	- Power consumption - High quality factor of LCTO (> 10) - Low K_{vco}
Disadvantages	- Poor quality factor of RO ($< \pi/2$) - Power consumption - High K_{vco}	- Silicon area used - Magnetic field sensitivity - Requires a RF process to integrate inductor with high Q

6 Conclusion

We have implemented a top down design process for low jitter PLLs. The layout of the circuit designed is presented on figure 17. The first step is to calculate the loop filter according to the parameters of the PLL, then to set the desired absolute jitter and optimize the VCO as a function of jitter. We did this for two types of PLL in order to compare the architecture with respect to the jitter, the power consumed and the silicon area. The absolute output jitter of both PLLs are less than 2 ps rms if internal couplings are reduced. Additionally, the silicon area of PLL_LC is three time higher than the PLL_RO, whereas the power consumption of the LCTO is 30% lower than the RO. Therefore, the trade-off between the rms absolute jitter, the power consumption and the silicon area will be the keys parameters when choosing the PLL architecture. The next steps are to reduce internal couplings, to optimize VCOs jitter and therefore to minimize output PLL jitter.

Acknowledgments

We would like to thank IN2P3 for the financial support and M. Idzik from AGH for providing the differential output driver.

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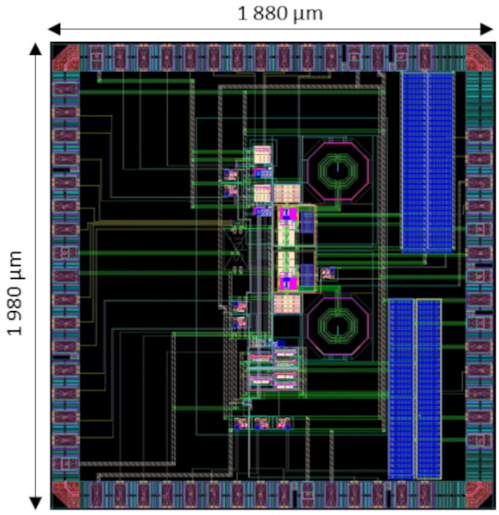

Figure 17. Layout of the designed circuit

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References

[1] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, *Comparison of a 65 nm CMOS ring- and LC-oscillator based PLL in terms of TID and SEU sensitivity*, *IEEE Trans. Nucl. Sci.* **64** (2017) 245.

[2] J. Prinzie, M. Steyaert, P. Leroux, J. Christiansen and P. Moreira, *A single-event upset robust, 2.2 GHz to 3.2 GHz, 345 fs jitter PLL with triple-modular redundant phase detector in 65 nm CMOS*, in *Proceedings of the IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Toyama, Japan, 7–9 Novemeber 2016, pp. 285–288.

[3] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, *Radiation tolerant, low noise phase locked loops in 65 nm CMOS technology*, *EPJ Web Conf.* **170** (2018) 01021.

[4] F. Lei and M.H. White, *Reference injected phase-locked loops (PLL-RIs)*, *IEEE Trans. Circuits Syst. I, Reg. Papers1* **64** (2017) 1651.

[5] B. Razavi, *A study of phase noise in CMOS oscillators*, *IEEE J. Solid-State Circuits* **31** (1996) 331.

[6] S.V. Shinde, *Review of Oscillator Phase Noise Models*, in *Proceedings of the International MultiConference of Engineers and Computer Scientists*, Hong Kong, China, 12–14 March 2014, Vol. II, pp. 733–740 [https://www.researchgate.net/publication/287019272_Review_of_Oscillator_Phase_Noise_Models].

[7] T. Lee and A. Hajimiri, *Oscillator phase noise: a tutorial*, *IEEE J. Solid-State Circuits* **35** (2000) 326.

[8] K. Kundert, *Predicting the Phase Noise And Jitter of PLL-Based Frequency Synthesizers*, Version 4i 23 october 2015, https://designers-guide.org/analysis/PLLnoise+jitter.pdf.

[9] K. Kundert, *Modelling Jitter in PLL-based Frequency Synthesizers*, Version 4h, March 2012, https://designers-guide.org/analysis/PLLjitter.pdf.

[10] J.A. McNeill, *Jitter in ring oscillators*, *IEEE J. Solid-State Circuits* **32** (1997) 870.

[11] J.A. McNeill, *Jitter in Ring Oscillators*, A.B, Dartmouth College, 1983, M.S.E.E. University of Rochester (1991), https://users.wpi.edu/~mcneill/papers/thesis.pdf.

2022 JINST 17 T05014

[12] X. Shi, *Design of Low Phase Noise Low power CMOS Phase Locked Loops*, Ph.D. thesis, Université de Neuchatel, Institut de Microtechnique, 2008, https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.634.6614&rep=rep1&type=pdf.

[13] D.C. Lee, *Analysis of jitter in phase-locked loops*, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.2* **49** (2002) 704.

[14] W.-H. Lee, J.-D. Cho and S.-D. Lee, *A high speed and low power phase-frequency detector and charge-pump*, in *Proceedings of the ASP-DAC '99 Asia and South Pacific Design Automation Conference*, Hong Kong, China, 21 January 1999, pp. 269–272.

[15] C. Hsu, K. Tripurari, S.-A. Yu and P.R. Kinget, *A 2.2 GHz PLL using a phase-frequency detector with an auxiliary sub-sampling phase detector for in-band noise suppression*, in *Proceedings of the IEEE Custom Integrated Circuits Conference*, San Jose, CA, U.S.A., 19–21 September 2011, pp. 1–4.

[16] L. Lin, L. Tee and P. Gray, *A 1.4 GHz differential low-noise CMOS frequency synthesizer using a wideband PLL architecture*, in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, San Francisco, CA, U.S.A., 9 February 2000, pp. 204–205.

[17] L. Romano, S. Levantino, S. Pellerano, C. Samori and A. Lacaita, *Low Jitter Design of a 0.35 µm-CMOS Frequency Divider Operating up to 3 GHz*, in *Proceedings of the 28th Solid-State Circuits Conference*, Florence, Italy, 24–26 September 2002, https://ieeexplore.ieee.org/document/1471601.

[18] W.S.T. Yan and H. Luong, *A 900-MHz CMOS low-phase-noise voltage-controlled ring oscillator*, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.2* **48** (2001) 216.

[19] C. Li and J. Lin, *A 1–9 GHz linear-wide-tuning-range quadrature ring oscillator in 130 nm CMOS for non-contact vital sign radar application*, *IEEE Microwave Wireless Compon. Lett.* **20** (2010) 34.

[20] D. Ham and A. Hajimiri, *Concepts and methods in optimization of integrated LC VCOs*, *IEEE J. Solid-State Circuits* **36** (2001) 896.

[21] P. Andreani, A. Bonfanti, L. Romano and C. Samori, *Analysis and design of a 1.8-GHz CMOS LC quadrature VCO*, *IEEE J. Solid-State Circuits* **37** (2002) 1737.

[22] W. Bae, *State-of-the-art circuit techniques for low-jitter phase-locked loops: Advanced performance benchmark FOM based on an extensive survey*, in *Proceedings of the IEEE International Symposium on Circuits and Systems*, Daegu, Korea, 22–28 May 2021, pp. 1–5.

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