FASTIME: A Multi-Channel 130 nm CMOS ASIC for a Complete Fast and High-Resolution Time Measurement Chain

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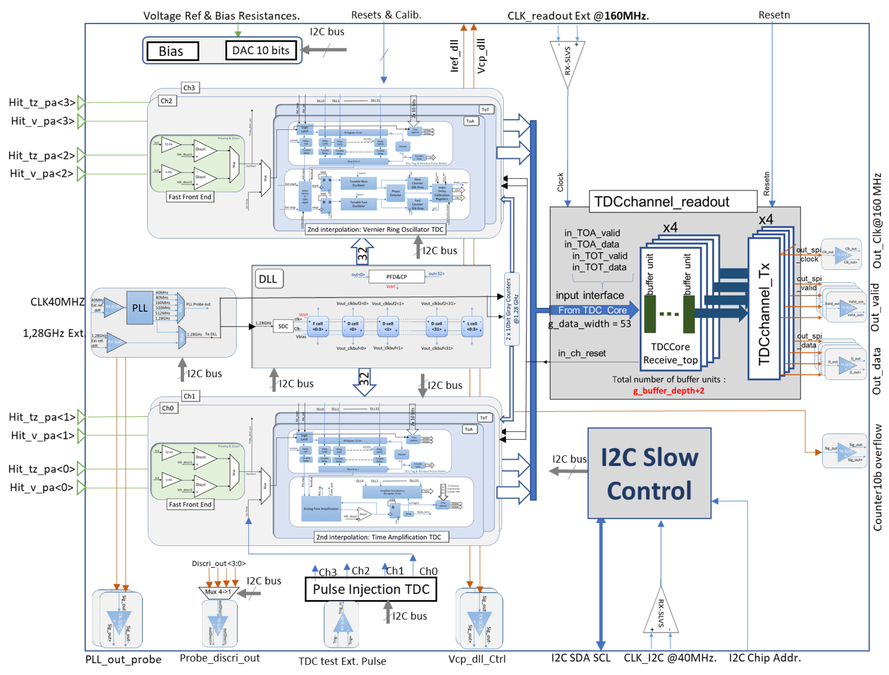
Poster Number: N-13-008

Motivations

FASTIME is a multi-channel ASIC providing a complete time measurement chain with a precision target of the order of 1 picosecond for 1 pC input charge and a dead time less than ten nanoseconds. Such resolution becomes necessary in various fields such as future particle physics experiments at FCChh to mitigate the expected pile-up of 1000, or in future generations of medical imaging (PET) to reduce significantly the dose injected into patients. It will also be needed to exploit a new type of sensors with high temporal resolution called NanoChannel Plate (NCP).

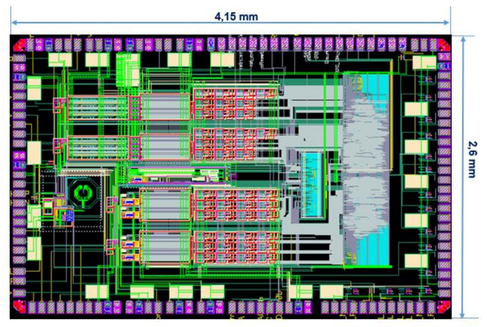
Circuit description

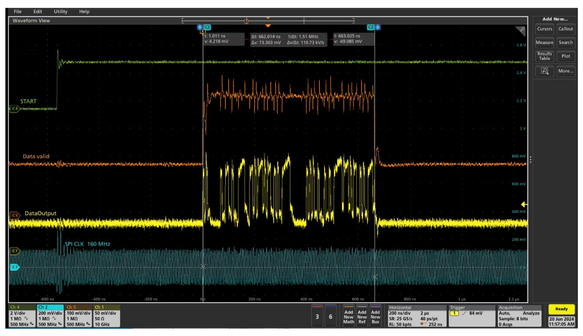
This prototype was produced in the 130 nm CMOS process. It consists of 4 channels; each one comprises a Fast Front End (FFE) stage coupled with a discriminator followed by a Time-to-Digital Converter (TDC) with double-level time interpolation. A 10-bit coarse counter provides 800 ns on-chip dynamic range. The first interpolation level of TDC is based on a Delay Locked Loop (DLL) with 32 differential delay elements operating at 1.28 GHz reference clock, which is generated by a sub-ps jitter on chip PLL, allowing a quantization step of 24.4 ps resulting in a theoretical accuracy of 7 ps rms. To refine the DLL temporal precision, a second level of time interpolation is added using two different TDC architectures, Vernier Ring-Oscillator TDC and a Time Amplifier TDC, both with an LSB of 3 ps. An intermediate circuit called Residue Pulse Maker generates the start and stop signals needed for the 2nd level interpolator. The FFE stage also integrates two preamplifier architectures: a Voltage Preamplifier and a Trans-Impedance one. The ASIC is fully configurable via slow Control (I2C). A digital readout block performs initial data processing and serializes TDC data in differential mode with an output clock of 160 MHz. Each channel measures both ToA and ToT, the latter is used to compensate for time walk.



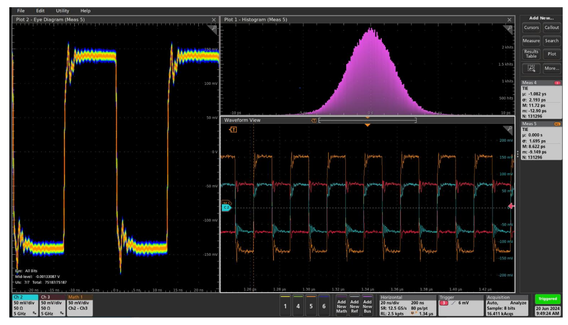
Test Results

The circuit was manufactured in early 2023 It occupies a 2.6x4.15 mm² area including PADs. Testing has progressed well. The qualification of this ASIC requires meticulous work in calibrating the oscillators of the Vernier TDC, the DNL of the DLL, and the parameters of the Residue Pulse Maker (timing of start & stop signals), as well as the gain factor of the time amplifier.



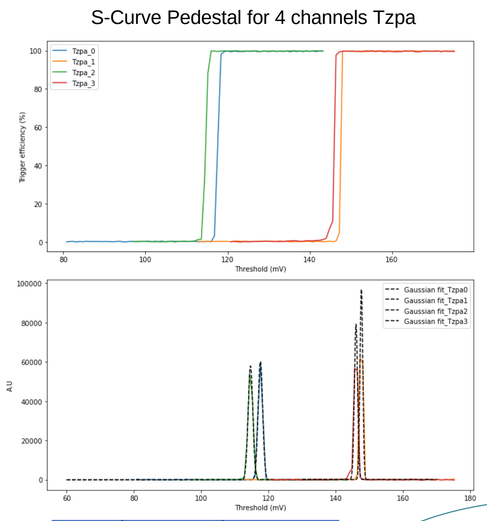


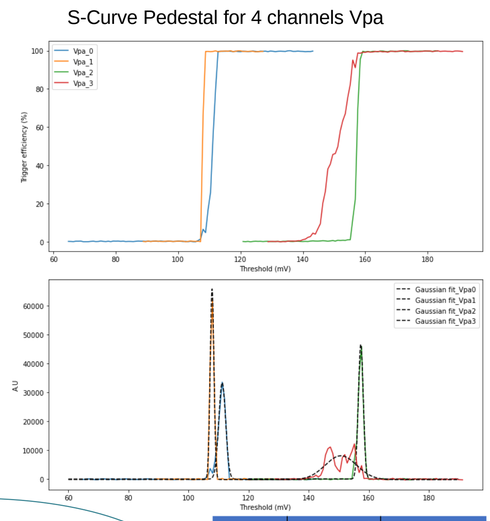
TDC output data frame: on a start signal, the TDC sends a 106-bit serial data signal including ToA and ToT, a DataValid signal as well as the serialization clock at 160 MHz. This plot demonstrates the good working of the whole chain.



PLL @ 1,28 GHz: The integrated PLL achieves 1.7 ps rms Jitter in test. This amount cumulates the Clock reference input jitter. The simulated jitter is less than 1 ps rms**.**

FFE&Discriminator test results

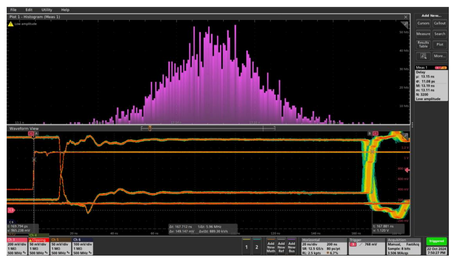




Tzpa	Mean (mV)	StdDev (mV)
0	117,5	0,479
1	147,58	0,292
2	114,63	0,488
3	145,9	0,340

The Transimpedance Preamp performs a slightly better result than Voltage Preamp.

Vpa	Mean (mV)	StdDev (mV)
0	111,2	0,81
1	107,8	0,441
2	157,3	0,58
3	150,7	3,70

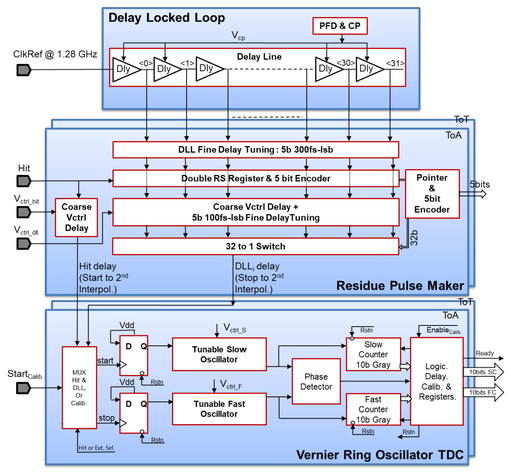


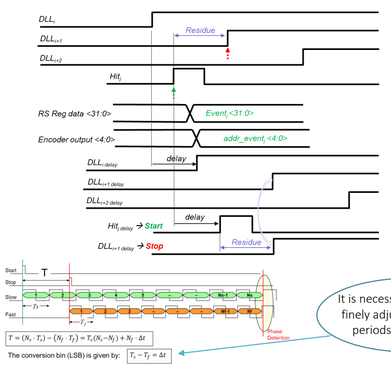
Jitter Channel 1: 11 ps rms Jitter for ToA of Voltage Preamp with 0,75 pC input Charge. The simulated jitter is less than 1 ps rms for 1 pC input**.**

Channel number	Tzpa Jiter (ps rms)	Vpa Jiter (ps rms)
0	24	13
1	20.7	11
2	21	13.5
3	19.5	12

Jitter of all channels: jitter of the Tzpa is less good, the injected charge is not entirely transmitted to the preamp. a part is lost in the parasitic capacities of the asic case

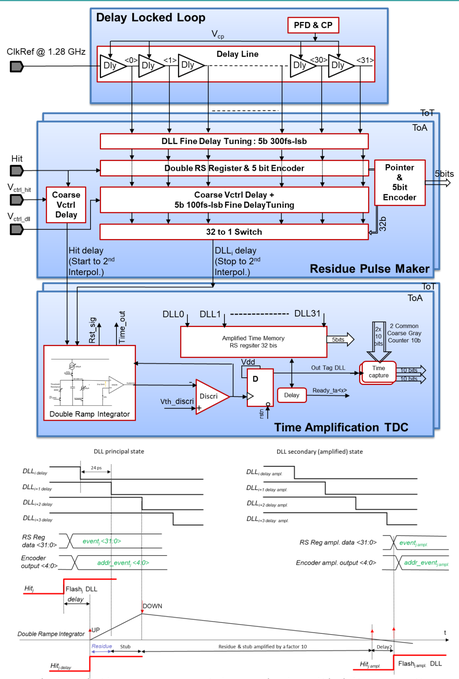
Vernier RO - TDC Working Principle





It is necessary to be able to finely adjust the oscillator periods by calibration

Time Amp - TDC Working Principle

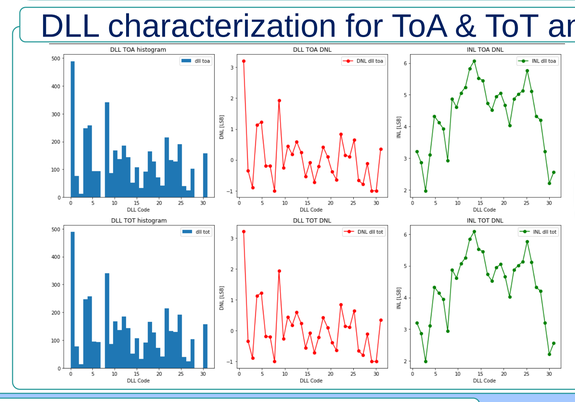


Temporal simulations: parametric analysis with hit every 2 ps

mesure	n0	code DLL principal	to hit	code DLL secondaire
mesure	244	25	1,04860-08	23
mesure	245	25	1,04880-08	22
mesure	246	26	1,04900-08	1
mesure	247	26	1,04920-08	0
mesure	248	26	1,04940-08	31
mesure	249	26	1,04960-08	30
mesure	250	26	1,04980-08	29
mesure	251	26	1,05000-08	28
mesure	252	26	1,05020-08	28
mesure	253	26	1,05040-08	27
mesure	254	26	1,05060-08	26
mesure	255	26	1,05080-08	25
mesure	256	26	1,05100-08	24
mesure	257	26	1,05120-08	24
mesure	258	27	1,05140-08	1
mesure	259	27	1,05160-08	1
mesure	260	27	1,05180-08	0

Set-up :
Time amplifier gain = 10
DLL lsb = 24 ps
→ from 12 to 13 codes for principal Time
→ de 1 à 2 codes for secondary Time

DLL characterization for ToA & ToT and Power budget

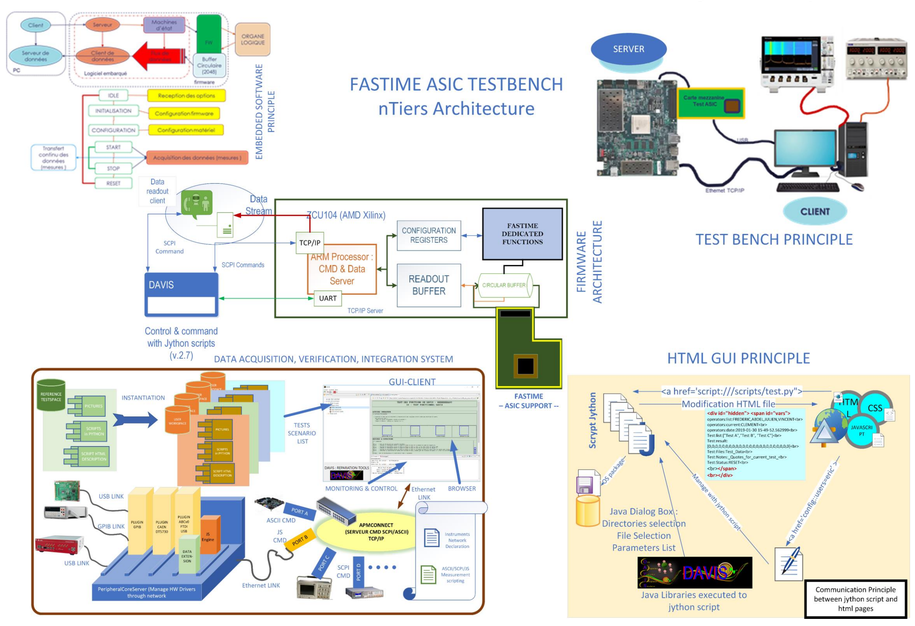


DLL preliminary results without correction. An integrated tuning system allows to correct the non-linearity.

Power Budget (VDD=1,2 V)	
Sub-block	Power dissipation
DLL	100 mW
PLL	13 mW
Vernir RO TDC (with RPM)	100 mW/ Ch
Time Amp. TDC (with RPM)	80 mW/ Ch
FFE: TzPa	9 mW
FFE: VPa	6 mW

Test Bench

The TB setup is based on an FMC mezzanine card paired with an AMD ZCU104 FPGA card for I2C control of the ASIC and SPI data acquisition. Embedded software running on the ARM microprocessor, developed in C, enables a TCP/IP server for Unicode commands. These commands allow for the configuration of ASIC registers and control of instruments associated with the tests. On the PC side, a client, following an n-tier architecture, enables the user to write test scenarios in Jython scripts



Conclusions and perspectives

The circuit is currently being tested. Preliminary test results are promising and validate all circuit functionalities and features. More detailed and exhaustive tests such as the noise, jitter, crosstalk, linearity, readout speed, testing set up and methods are in progress.

Dedicated software is being developed to automate tests and carry out statistical studies. A human machine interface was designed using DAVIS (Data Acquisition, Verification, Integration System) software to facilitate interaction with the different design blocks.

The FFE jitter is higher than simulated values, we are exploring the possible causes and sources of this degradation. A new version of analog mezzanine test bord has been designed, the asic will be directly wire bonded without any packaging in order to reduce input capacitors, wire bonding self etc.

In this design, all blocks can be tested separately. TDCs can be tested directly with an external trigger signal, in order to isolate the performance of the TDC from the impact of the FFE jitter.

References

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[3] L. S. de Paula, et al. "A wide band CMOS differential voltage-controlled ring oscillator," 2008 Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference, Montreal, QC, Canada.